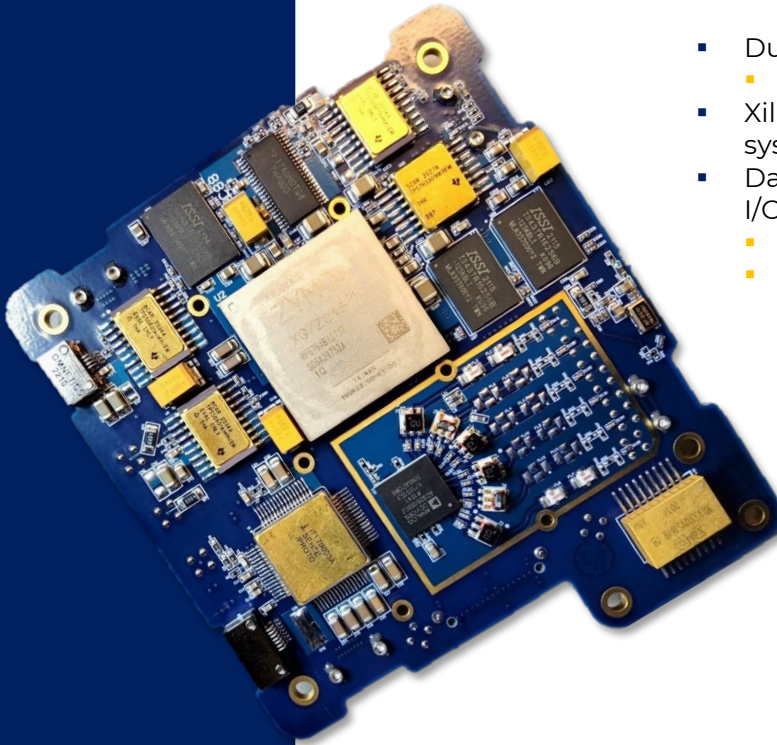


ASTROSDR-G SDR AND DSP SYSTEM FOR SPACEFLIGHT



- Dual receivers & transmitters
 - 70 MHz to 6 GHz
- Xilinx Zynq Z-7045 FPGA & dual ARM system-on-chip (SoC)
- Daughter card interface for expansion, I/O, and custom applications
 - 64 Gbyte eMMC flash memory card
 - Gigabit Ethernet and flash memory card with GPIO

THE ASTROSDR-G provides key components for a user-developed RF payload: receiver, transmitter, FPGA, ARM processor, data storage, and high-speed I/O. The board-support-package includes pre-build functions for interfacing to the radio, ARM processor, and eMMC storage, as well as a Vivado project to assist the user in developing their own unique applications.

ASTROSDR-G HAS THE DEVELOPER-FRIENDLY FEATURES

found in our terrestrial SDR and DSP systems. The onboard processor runs embedded Linux, providing a flexible and capable development environment. APIs are provided for basic control of the FPGA, receivers, and transmitters.

ASTROSDR-G HAS MULTIPLE INTERFACES for I/O and command/control: dual UARTs, buffered SpaceWire (4 LVDS pairs), and an Ethernet interface on an optional daughter-card.

RINCON RESEARCH SUPPORTS MISSIONS with more than just hardware. We provide mission planning and operation services. We also have unique IP for digital signal processing, including interference cancellation, high-rate modems, adaptive beamforming, geolocation, and space situational awareness.

ORDERING INFORMATION

PART NUMBER

- Flight Grade: ASDR-RF-G

EXPORT CONTROLS

- ECCN: 9A515

SPECIFICATIONS

PROCESSING

- Xilinx Zynq 7045 FPGA and dual ARM SoC
- ARM Resources:
 - Dual-core Arm Cortex A9 with NEON, up to 733 MHz
 - Attached 512 MByte DDR3 RAM (with ECC)
 - Attached 2 GByte flash for radiation-tolerant OS storage
- FPGA Resources:
 - 350k logic cells
 - 900 DSP slices
 - Attached 1 GByte DDR3 RAM (ECC capable)

MECHANICAL

- 90 mm x 102.2 mm
- Approximately 100 grams (without heatsink or daughter card)

ENVIRONMENTAL

- Operating Temp: -25°C to 60°C
- Radiation test results available by request

POWER

- Power: 7 VDC to 13 VDC
- Idle: 4 W (typ)
- Max: 30 W, 16A available for the VCCINT FPGA core voltage

DIGITAL INTERFACES

- CAN:** Microcontroller connected and bus powered
 - Remote on/off capable
 - 9-pin nano-D connector (2x for pass-through)
- Timing Signals:** FPGA connected
 - 1 PPS
 - Serial timecode (DC-IRIG-B) (MMCX)
 - Internal 50 MHz reference oscillator
- Daughter Card Interface:** 30 pins 1.8 V GPIO (includes 11 ADC channels)
 - 24 pins 3.3 V GPIO
 - Samtec LSHM-130 60-pin strip, available for connections to custom board or cables
- SpaceWire:** FPGA connected, 4-LVDS pairs up to 200 MHz operation (or 8 GPIO)
 - 9-pin nano-D connector
- Development Interface:** External watch dog timer input, Reset, JTAG, UART console
 - 15-pin nano-D connector

ADDRESS

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