ASTROSDR
SDR AND DSP SYSTEM FOR SPACEFLIGHT

- Dual receivers & transmitters, 70 MHz to 6 GHz
- AMD Zynq Z-7045 FPGA & dual ARM SoC
- Daughter card interface for expansion, I/O, and custom applications
    - 64-Gbyte eMMC flash memory card
    - Gigabit Ethernet and flash memory card with GPIO
- 64-GByte embedded Multi-Media Card (eMMC) flash on daughter card for data storage

ASTROSDR

THE ASTROSDR PRODUCT FAMILY

- Provides key components for a user-developed RF payload: receiver, transmitter, FPGA, ARM processor, data storage, and high-speed I/O
- Includes a board support package with pre-build functions for interfacing to the radio, ARM processor, and eMMC storage, as well as a Vivado project to assist users in developing their own unique applications

ASTROSDR DEVELOPER-FRIENDLY FEATURES

- Developer-friendly features are found in our terrestrial software-defined radio (SDR) and digital signal processing (DSP) systems
- Onboard processor runs embedded Linux, providing a flexible and capable development environment
- APIs are provided for basic control of the FPGA, receivers, and transmitters

ASTROSDR MULTIPLE INTERFACES

- Multiple interfaces are included for I/O and command/control: dual UARTs, two FPGA-attached low-voltage differential signaling (LVDS) pairs, and an Ethernet interface on an optional daughter card

RINCON RESEARCH SUPPORTS MISSIONS

- More than just hardware, we provide mission planning and operation services
- We have unique IP for digital signal processing, including interference cancelation, high-rate modems, adaptive beamforming, geolocation, and space situational awareness

BLOCK DIAGRAM

AstroSDR

Legend:
- Radiation Hardened
- Defense Grade
- Industrial Grade
- Connectors
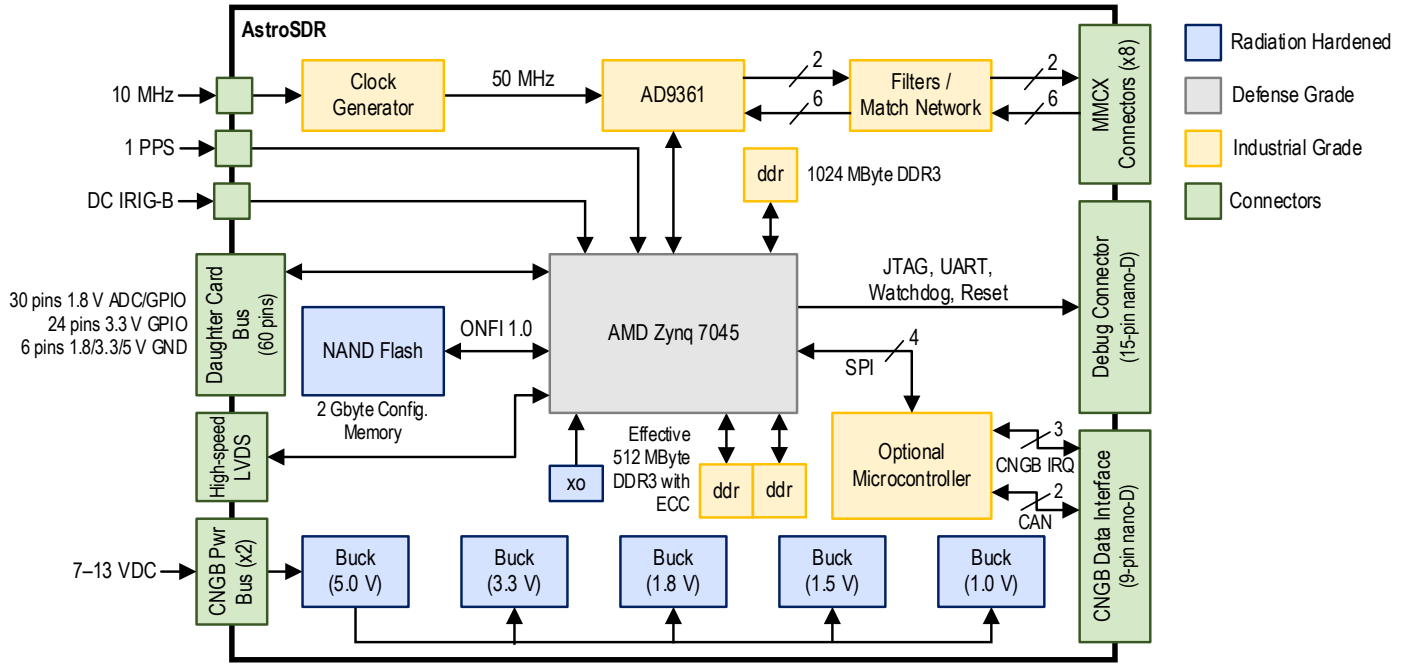
SPECIFICATIONS

PROCESSING
- ARM Zynq 7045 FPGA and dual ARM SoC
- ARM Resources:
    - Dual-core ARM Cortex A9 with NEON, up to 733 MHz
    - Attached 512-MByte DDR3 RAM (with ECC)
    - Attached 2-GByte flash for radiation-tolerant OS storage
- FPGA Resources:
    - 350 k logic cells
    - 900 DSP slices
    - Attached 1-GByte DDR3 RAM (ECC capable)
    - Attached 64-GByte eMMC flash on daughter card, designed to support dual-channel recording at up to 8 MS/s (32 Mbytes/s)
    - Each eMMC supports sustained write speeds of 8 Ms/s

MECHANICAL
- 90 mm x 90 mm (3.543" x 3.543")
- Approximately 95 grams (without heatsink or daughter card)

ENVIRONMENT
- Operating temp: –25° C to 60° C (flight), 0° C to 60° C (eng.)
- Vibration: Passed GEVS proto-qualification levels
- Thermal vacuum: –20° C to +50° C operational
- 5+ years of on-orbit heritage, more info available upon request

POWER
- Power: 12 VDC
- System management: 3.5 W (no FPGA load, ARM booted)
- Idle: 4 W
- Passive collect: 5.5 W (includes recording to flash)
- Max: 30 W 6A available for 0.85V FPGA VCC_INT rail

DIGITAL INTERFACES
- **GPIO/SPI/I2C:**
    - 9-pin nano-D connector (2x for pass-through)
- **Timing Signals:** FPGA connected
    - 1 PPS, 5/10/50 MHz reference (MMCX)
    - Serial timecode (DC-IRIG-B) (MMCX)
- **Daughter Card Interface:**
  30 pins 1.8 V GPIO (includes 11 ADC channels)
    - 24 pins 3.3 V GPIO
    - Samtec LSHM-130 60-pin strip, available for connections to custom board or cables
- **LVDS:** FPGA connected, 4-LVDS pairs up to 200 MHz operation (or 8 GPIO)
    - 9-pin nano-D connector
    - Supports HDLC (transmit only)
    - Supports SpaceWire link layer
- **Development Interface:**
  External watch dog timer input, reset, JTAG, UART console
    - 15-pin nano-D connector
    - **ECCN 9A515**

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EMPLOYEE OWNED